AMENDMENTS TO THE DRAWINGS

Attached hereto are three (3) sheets of corrected formal drawings. The corrected formal drawings incorporate the following drawing changes:

In Figs. 1-3, the reference numerals 117 and 125 are added to respectively designate the output of the second delay processing unit 107 and the output of the first delay processing unit 106.

In Fig. 3, the reference numeral "312" has been added to replace the original reference numeral "215."

REMARKS

Applicant appreciates the Examiner's thorough consideration provided the present application. Claims 4, 5 and 7 are now present in the application. The specification, drawings, and claims 4, 5 have been amended. Claim 7 has been added. Claims 1-3 and 6 have been cancelled. Claims 4 is independent. Reconsideration of this application, as amended, is respectfully requested.

Specification Objections

The specification and title have been objected to due to its non-descriptiveness. In view of the foregoing amendments, it is respectfully submitted that the objection to the title has been addressed.

In addition, Applicant respectfully submits that the specification on page 5 is consistent with the specification on page 7 with regard to the functions of parts 201 and 213-215, since both recite "The first left channel output signal 131 and the first right channel output signal 13 are further mixed at the subtracter 213 and then processed by the third gain unit 201. The output of the third gain unit 201 is subtracted from the first left channel output signal 131 by the fourth subtracter 214 to produce a second left channel output signal 231. Similarly, the output of the third gain unit 201 is subtracted from the first right channel output signal 132 by the fifth subtracter 215 to produce a second right channel output signal 232." which is for clarifying the combination of those parts. In addition, the subtracter(s) can be an adder(s), because both have the same circuitry.

Reconsideration and withdrawal of this objection are respectfully requested.

Drawings Objections

The drawings have been objected under 37 C.F.R. § 1.84(p)(5). Applicant has submitted three (3) sheets of corrected formal drawings to address the Examiner's requested changes and to further clarify the invention. Reconsideration and withdrawal of this objection are respectfully requested.

Claim Rejections Under 35 U.S.C. §112

Claims 1-6 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Claims 5 and 6 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. These rejections are respectfully traversed.

In view of the foregoing amendments, it is respectfully submitted that these rejections have been addressed. Accordingly, all pending claims comply with the enablement requirement and are now definite and clear. Reconsideration and withdrawal of the rejections under 35 U.S.C. § 112, first and second paragraphs, are therefore respectfully requested.

Claim Rejection Under 35 U.S.C. § 103

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jyosako, U.S. Patent No. 5,657,391. This rejection is respectfully traversed.

In light of the foregoing amendments to the claims, Applicant respectfully submits that this rejection has been obviated and/or rendered moot. As the Examiner will note, independent claim 4 has been amended.

Independent claim 4 has been amended to recite a combination of elements including "a first gain unit receiving and processing the left channel audio signal; a high pass filter processing unit coupled to the first gain unit; a first low-pass filter processing unit coupled to the first high-pass filter processing unit; a first delay processing unit coupled to the first low-pass filter processing unit; a second gain unit receiving and processing the right channel audio signal; a second high-pass filter processing unit coupled to the second gain unit; a second low-pass filter processing unit coupled to the second high-pass filter processing unit; a second delay processing unit coupled to the second low-pass filter processing unit; a first subtracter coupled between the first high-pass filter processing unit and the second delay processing unit, subtracting the output of the second delay processing unit from the output of the first high-pass filter processing unit; and a second subtracter coupled between the second high-pass filter processing unit and the first delay processing unit, subtracting the output of the first delay processing unit from the output of the second high-pass filter processing unit; wherein the first and the second gain units are used to prevent the first and the second high-pass filter processing units from being saturated."

Applicant respectfully submits that the above combination of elements as set forth in amended independent claim 4 are not disclosed nor suggested by the reference relied on by the Examiner.

Jyosako is directed to a sound image enhancement apparatus, which is used for reproducing two-channel stereo signals with speakers. Jyosako's apparatus includes a first phase

shifter and a second phase shifter for introducing different amounts of phase shift to the signals. These shifters enable virtual speakers to be located at the back of a listener. Furthermore, an FIR filter is also used for simulating sound fields at a live performance.

Although Jyosako is used to simulate sound fields, Jyosako nowhere discloses the claimed features provided by the gain units – including the first gain unit (e.g., element 100 illustrated in the embodiment) and the second gain unit (element 101 illustrated in the embodiment) used to prevent the high-pass filter processing unit from being saturated as recited in claim 4. More, the claim 4 further features that the provided first/second subtracter is used to subtract the output of the second/first delay processing unit from the output of the first/second high-pass filter processing unit, that is what the Jyosako fails to teach.

Since Jyosako fails to teach each and every limitation of amended independent claim 4, Applicant respectfully submits that claim 4 and their dependent claims clearly define over the teachings of Jyosako. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103 are respectfully requested.

Additional Claim

Claim 7 has been added for the Examiner's consideration. Applicant respectfully submits that claim 7 depends, either directly or indirectly, from independent claim 4, and is therefore allowable based on its dependence from independent claim 4, which is believed to be allowable. Favorable consideration and allowance of claim 7 are respectfully requested.

CONCLUSION

It is believed that a full and complete response has been made to the Office Action, and that as such, the Examiner is respectfully requested to send the application to Issue.

In the event there are any matters remaining in this application, the Examiner is invited to contact Joe McKinney Muncy, Registration No. 32,334 at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Dated: December 26, 2007

Respectfully submitted,

By _____
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Attachment: Replacement sheets